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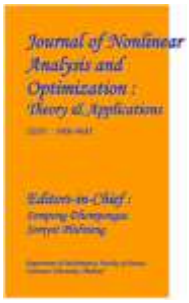

A Hybrid Technique to Build a Dynamic Comparator with High Speed and Low Power

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ABSTRACT ***A low-power comparator is presented. pMOS transistors are used at the input of the preamplifier of the comparator as well as the latch stage. Both stages are controlled by a special local clock generator. At the evaluation phase, the latch is activated with a delay to achieve enough preamplification gain and avoid excess power consumption. Meanwhile, small cross coupled transistors increase the preamplifier gain and decrease the input common mode of the latch to strongly turn on the pMOS transistors (at the latch input) and reduce the delay. Unlike the conventional comparator, the proposed structure let us set the optimum delay for preamplification and avoid excess power consumption. The speed and the power benefits of the comparator were verified using solid analytical derivations process–VDD temperature corners, and Monte Carlo simulations along with silicon measurements in 0.18 µm. The tests confirm that the proposed circuit reduces the power consumption by 50% and provides 30% better comparison speed at the same offset and almost the same noise budgets. Moreover, the comparator provides a rail-to-rail input Vcm range in fclk = 500 MHz.***

Index Terms: ***Dynamic comparator, high speed, low-offset comparator, low power, two-stage comparator***

1.INTRODUCTION

Now a days, a low power high speed ADCS are integral parts of a variety of applications such as hand-held devices. Comparators are the key building blocks of different types of ADCs, such as SAR, pipeline, and flash ADCs [1] – [4]. Several years ago, CMOS

amplifiers were used as static comparators, although they suffer from very high-power consumption (since they are always on) and inherent limited speed (since they have no positive feedback) [1]. Dynamic comparators improve the speed and reduce the total power consumption of the static comparators, since they employ positive feedback and save static power consumption [5]. One-stage dynamic comparators were proposed which used a latch circuit cascaded with a pre amplifier. The kickback noise which is caused through the capacitive path from the output to input nodes makes the one-stage dynamic comparators inferior choices compared to their two stage counterparts [6]. In the two-stage dynamic comparators, the problem of kickback noise is improved by weakening the capacitive path. In fact, in the two-stage dynamic comparators, the capacitive path is comprised of the series connection of gate–drain (*C*GD) capacitors [6]. In the two-stage dynamic comparators, the first stage amplifies the input differential signal and is called the preamplifier stage while the second stage, the latch stage, amplifies its input differential signal up to VDD at one side and GND at the other side [1] – [7].

Examples of the two-stage dynamic comparators can be widely found in the literature. In the comparator reported in [8], the connection of the first stage to the second stage improves the speed and area, although a high-speed criterion causes offset and significant power consumption. In addition, the direct connection of the output nodes of the first and second stages (which endure a large voltage swing) deteriorates the kick back noise [6]. Two-stage comparators need both clock and its inverted signal to perform a comparison, which ask for a stricter timing design. To cover this problem, the comparator of [9] is proposed in which the activation of the latch is made by the common-mode voltage of the output nodes of the preamplifier, so it works with only one clock signal. Besides, the pMOS transistors are used at the input of the comparator to use their bulk pins for offset cancellation. Using this technique, the offset voltage is reduced at the cost of speed reduction. In that work, considering a low offset voltage, small sizing can be used for the input transistors of the preamplifier to reduce the power; however, the power is still high due to the additional components. In [10], a comparator with nMOS input transistors is reported to improve the speed; however, it increases the power consumption by a factor of four, since the preamplifier stage is always on to enhance the speed [10]. The comparator presented in

[11] uses combined preamplifier and latch stages. The latch is activated with a delay to reduce the power consumption, achieving an acceptable offset voltage. However, it suffers from larger kickback noise and higher transistor count compared to the conventional method. In [12], a two-stage comparator is proposed which uses a simple latch with a direct connection to the output nodes of the preamplifier. This comparator is also working with a delayed clock to improve the offset voltage; however, it degrades the speed. Moreover, it suffers from kickback noise which is originated from the direct connection of the output nodes of the first and second stages. Moreover, using large input transistors for a low offset voltage result in large parasitic capacitors at the output nodes of the preamplifier stage. This capacitor must be charged using the latch stage; therefore, higher power consumption is required. The methods reported in [21] – [27] are some of the recent innovations on the dynamic comparators. For example, in [27], a low-power comparator with cross-coupled circuit is proposed which exacerbates the offset voltage, area. Also, the kickback noise increases since the preamplifier suffers a fast rail–rail voltage swing.

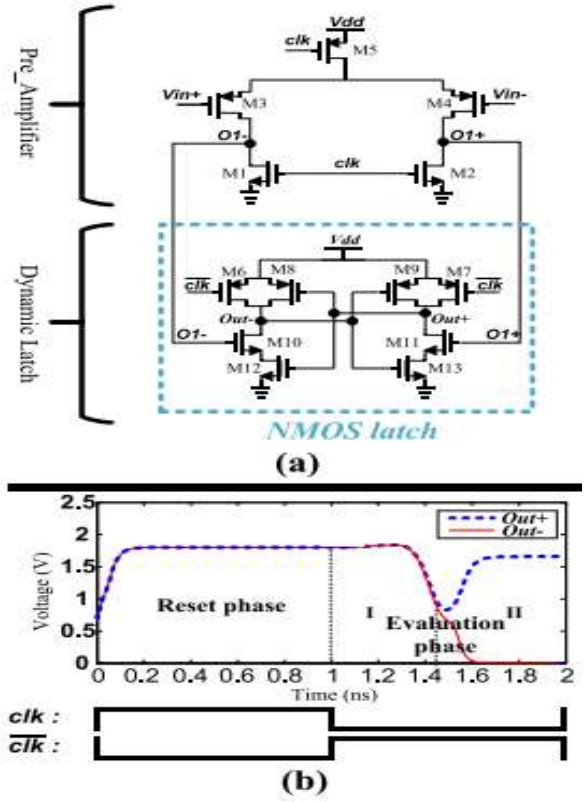
In this paper, a special controller (local clock generator) for the comparator and pMOS latch with pMOS preamplifier (latch and preamplifier with input pMOS transistors) are presented to achieve low-power and high-speed benefits. It is shown that the proposed comparator reduces the power consumption by half while increasing the speed. Moreover, it operates at large input common-mode voltages close to VDD, although pMOS transistors are used at the input of the comparator. As another benefit, the preamplification delay can be set to its optimum value to have a better comparison speed and reduce excess power consumption. However, in the conventional and other comparators, this delay is fixed to a value which is far from its optimum point. As a result, the proposed comparator is a good candidate for precise low power high-speed applications.

2.CONVENTIONAL SYSTEM

Below figure presents the two-stage version of the conventional dynamic comparator [5], [13]. This comparator is comprised of a preamplifier and a latch. At the first phase which is called reset phase, clk is set to “1” and clk is set to “0” to reset the first and second stages of the comparator to GND and VDD, respectively

(avoiding hysteresis). Then, clk changes to "0" and clk changes to "1" to begin the evaluation phase. ¯In this phase, the parasitic capacitors of the output nodes of the preamplifier begin to being charged differentially based on the input differential signal *(V*in+ - *V*in-*)*. When the common voltage at the output of the preamplifier becomes higher than the threshold voltage of an nMOS transistor (*M*10,11 in Fig. 1), the latch is turned on and amplifies its input differential voltage until it provides a rail-to-rail differential signal. In fact, the latch employs a positive feedback circuit to provide a fast amplification. Simultaneously, the output voltages of the preamplifier are charged to VDD.

Conventionally, for high-precision applications the size of the input transistors (*M*3,4) is chosen large enough to achieve a high preamplifier gain and a better transistor matching. In this case, the effect of the latch on the input referred offset voltage is negligible. As discussed earlier, during the evaluation phase the output voltages of the preamplifier are charged to VDD gradually. As a result, considering the large sizing of *M*3 and *M*4 which causes large parasitic capacitors(a) Conventional two-stage dynamic comparator. (b) Its typical output waveform and clock signal.at O1+ and O1- nodes, a low-offset comparator demands ahigh power consumption. In addition, the speed is limited to the speed of the latch. In addition, a longer time is required to charge the output voltages of the preamplifier stage to a level higher than an nMOS threshold voltage. In fact, during the evaluation phase the latch stage is not activated until the output voltages of the first stage are large enough to turn on the input nMOS transistors of the latch. Unfortunately, this delay is uncontrollable and varies with the input *V*cm of the comparator. Moreover, when the latch starts working the speed is low, since the overdrive voltage of *M*10,11 is almost zero and takes time to increase.



(a) Conventional two-stage dynamic comparator.
(b) Its typical output waveform and clock signal.

LITERATURE SURVEY

Design techniques for high-speed, high-resolution comparators

Precision techniques for the design of comparators used in high-performance analog-to-digital converters employing parallel conversion stages are described. Following a review of conventional offset cancellation techniques, circuit designs achieving 12-b resolution in both BiCMOS and CMOS 5-V technologies are presented. The BiCMOS comparator consists of a preamplifier followed by two regenerative stages and achieves an offset of 200 mu V at a 10-MHz clock rate while dissipating 1.7 mW. In the CMOS comparator offset cancellation is used in both a single-stage preamplifier and a subsequent latch to achieve an offset of less than 300 mu V at comparison rates as high as 10 MHz, with a power dissipation of 1.8 mW.

3.PROPOSED SYSTEM

The proposed comparator is shown in Below Fig. In contrast to the conventional comparator, a pMOS latch (a latch with input pMOS transistors) is used in the latch which is activated with a predetermined delay during the evaluation phase [*t*amp, as shown in Fig. (b)]. This delay is supposed to be the optimum delay. At the reset phase, the clk, clkb1, and clkb2 hold a logic "1" to discharge the output voltages of both preamplifier and latch to GND. At the evaluation phase, first the clk and clkb1are toggled to logic "0" to start preamplification (charging the parasitic capacitors of O1+ and O1- nodes differentially). During this phase, the cross-coupled circuit increases the differential voltage (***V***idl = [*V*O1+-*V*O1-]*)* slowly (since *M*4,5are mostly in subthreshold region) and reduces the common mode voltage (***V***cml = 0.5 × [*V*O1+ + *V*O1-]*)* to provide a strong drive

for the input pMOS latch stage. Increasing *V*idl (means larger preamplifier gain) further eliminates the effect of the latch on the input referred offset voltage. Also, larger *V*idl results in a smaller latch delay. Meanwhile, *V*cml is kept reducing by *M*3-5. The control signals are implemented using a local clock generator as shown in Fig. 2(b), which consumes a small amount of power. The black inverter is designed carefully to adjust the delay. Instructively, the proposed comparator is robust against overlapped control signals, since overlapped signals only slightly affect the power consumption and have no effect on the precision.

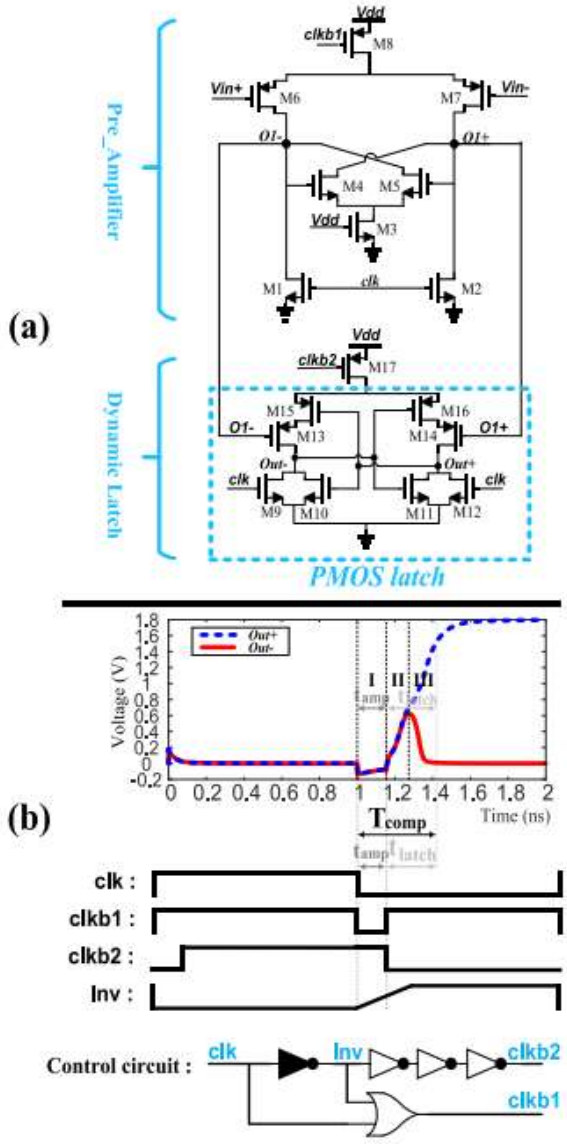


Fig.. (a) Proposed two-stage dynamic. (b) Its typical output waveform and clock signal.

In the proposed circuit, the delay of the evaluation-phase is long enough to achieve the minimum required preamplification gain for a given speed and latch offset elimination. Thanks to the cross-coupled circuit (*M*3-5*)*, during the first step of the evaluation phase, the differential voltage at O1+ andO1-nodes increases;

however, the common-mode voltage of those nodes is kept low. Therefore, for a sufficient evaluation phase delay, *t*amp, *V*cml (= 0.5 × [*V*O1+ + *V*O1-]*)* is pulled down to activate the pMOS latch strongly. Also, the larger *V*idl boosts the latching process (speed). Consequently, the delay of the comparator will be small and almost flat over a wide range of the input *V*cm. Transition of clkb1 to logic "1" limits the power consumption of the preamplifier which is the main part of the total power consumption. In the meanwhile, the cross-coupled circuit continues preamplification at no cost of power consumption.

As another benefit, the delay time from beginning of the evaluation phase to beginning of the latching process is simply controllable and can be tuned at its optimum value. However, in the conventional comparator, delay is inevitably fixed to the required time to charge the output parasitic capacitors of the preamplifier to the level of an nMOS voltage threshold. The proposed structure can also be implemented using nMOS transistors, i.e., latch and preamplifier with input nMOS transistors. This will result in a higher speed because of the inherent superiority of nMOS transistors over pMOS ones. The size of *M*4,5 is chosen large enough to keep the output common-mode voltage of the preamplifier small enough and increase the preamplifier differential gain. In this paragraph, the core concept of the proposed comparator is briefly described. In the conventional comparator, if the preamplifier and the latch work in different time slots, the power consumption is improved. To do this efficiently, one way is to change the structure of the conventional comparator from "pMOS preamp|| nMOS latch" to "pMOS preamp||pMOS latch" (or "nMOS preamp|| nMOS latch" for a better speed). In fact, the type of both the input transistors of the preamplifier and latch must be the same in contrast to general structure of the dynamic comparators [1]–[22]. The proposed pMOS–pMOS (nMOS–nMOS) structure requires a special clocking pattern to work correctly and efficiently. We develop a low-power small-area delay-line-based controller which in addition to controlling the comparator, it makes the comparator robust against process–VDD–temperature (PVT) variations since the delay of the controller and the delay of the comparator components varies in the same direction in different PVT corners. The preamplification delay can beset to achieve the optimum delay and this delay is almost optimum in all PVT corners.

In the achieved structure, Fig.1 without the cross-coupled circuit, the optimum delay could

not be realized since a larger preamplification time reduces the *V*GS voltage of the following input pMOS transistors of the latch (worsening the speed and power). Therefore, a circuit which reduces the input common-mode voltage of the pMOS latch is needed while (at least) it keeps the differential gain untouched. The cross-coupled circuit can do this. The size of the transistors is much smaller than the size of the input transistors of the preamplifier (about 7–10 times). Therefore, the power, area, and offset contribution of the cross-coupled

circuit is negligible. The cross-coupled circuit increases the differential voltage mainly when the preamplifier is turned off and enhances the speed; however, its main purpose is to reduce the input common-mode voltage of the latch.

$$\begin{cases} V_{cm} = \dfrac{V_{in+} + V_{in-}}{2} \\ V_{id} = V_{in+} - V_{in-}. \end{cases} \quad (3)$$

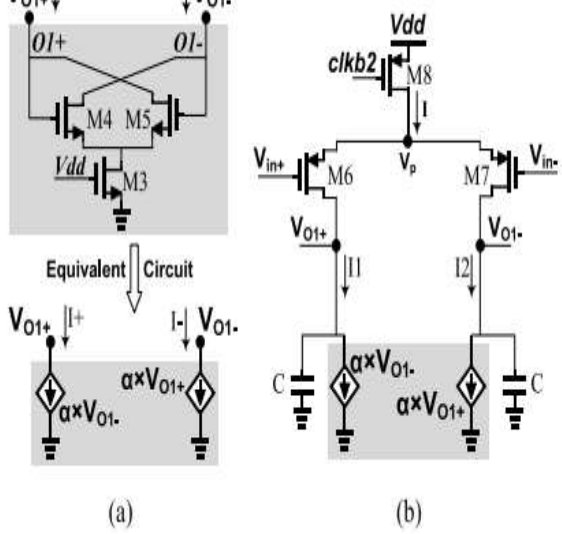


Fig. (a) Equivalent circuit of the cross-coupled part.
(b) Simplified circuit diagram of the preamplifier.

B.OffsetVoltage

The offset voltage is dependent on *V*cm, since the working region of the transistors changes and the nonideal effects such as channel length modulation alters the effect of mismatch of each component on the differential gain. The offset voltage of the comparator is calculated analytically for *V*cm less than VDD/2, where *M*6,7,8 work in the saturation region and the channel length modulation of *M*6,7 is negligible. In order topropose a closed-form equation, weneglect the effect of thelatch on the offset voltage (which is satisfied in a

good design).

As discussed earlier, in a good design the sizing of the input transistors (*M*6,7*)* for high-resolution applications are chosen large enough to eliminate the effect of the latch stage on the input referred offset voltage. Technically, the input referred dynamic offset is the input differential voltage (*V*in+-*V*in-*)* that establishes equal voltage at the O1+ and O1- nodes at the end of the preamplification phase *(t*amp*)*. The current of *M*6,7 [Fig. 3(b)] and the difference between them are calculated as follows by taking into account Based on the definition of the offset voltage, if an input differential voltage as large as *V*os is applied to the comparator,

*V*O1+ will be equal to *V*O1- after the amplification time (*t*amp*)*.Therefore, by solving the equation *V*O1+ = *V*O1- and substituting (11), the offset voltage is calculated in (13), shown at the bottom of this page.Fig. presents the simulation results of the offset voltage for the proposed comparator. In Fig. 5, the offsetvoltage versus *V*cmis shown considering 1 k-points SpectreMonte Carlo simulations (using 0.18-μm technology) and100 k-points MATLAB Monte Carlo simulations using (13).

IV.NOISE

In two-stage dynamic comparators, the offset voltage andsimilarly the input referred noise is mainly dominated bythe preamplifier stage. Using the proposed technique, bothinput nMOS and input pMOS preamplifiers can be used;their structures are similar to the conventional counterparts

PARAMETERS OF THE CONTROLLER IN DIFFERENT CORNERS

VDD = 1.6V									
Condition	$T = 0^oC$			$T = 27^oC$			$T = 70^oC$		
	ss	tt	ff	Ss	tt	ff	ss	tt	ff
Delay (ps)	230	175	133	246	185	140	270	201	152
Power (uW)	15	16	19	16	17	20	16	17	21
VDD = 1.8V									
Condition	$T = 0^oC$			$T = 27^oC$			$T = 70^oC$		
	ss	tt	ff	ss	tt	ff	ss	tt	ff
Delay (ps)	186	146	148	198	155	121	179	170	132
Power (uW)	20	22	26	21	23	27	22	24	27
VDD = 2V									
Condition	$T = 0^oC$			$T = 27^oC$			$T = 70^oC$		
	ss	tt	ff	ss	tt	ff	ss	tt	ff
Delay (ps)	156	126	102	166	134	108	183	146	117
Power (uW)	26	29	33	27	30	34	28	31	35

[neglecting the cross-coupled circuit Fig. 3(a)]. As a result, weexpect an almost equal input referred noise. In the proposedcomparator, the cross-coupled circuit increases both the noiseand the preamplification gain. On the other hand, the crosscoupled circuit keeps the output voltages of the preamplifierstage low so it keeps the preamplifier input transistors in the saturation region. This is in contrast to the conventionalcomparator where the input

transistors go to the triode regionduring preamplification exacerbating the input noise (gain ↓⇒*V*noise-in ↑*)*. Assuming all above, the first effect increasesthe input noise while the second one reduces the input noise.Therefore, totally, it is expected that the input noise of the proposed comparator will be almost the same as the conventionalcomparator. In Section VI, multiple transient noise simulationsprove this inspection.

Corner Simulations

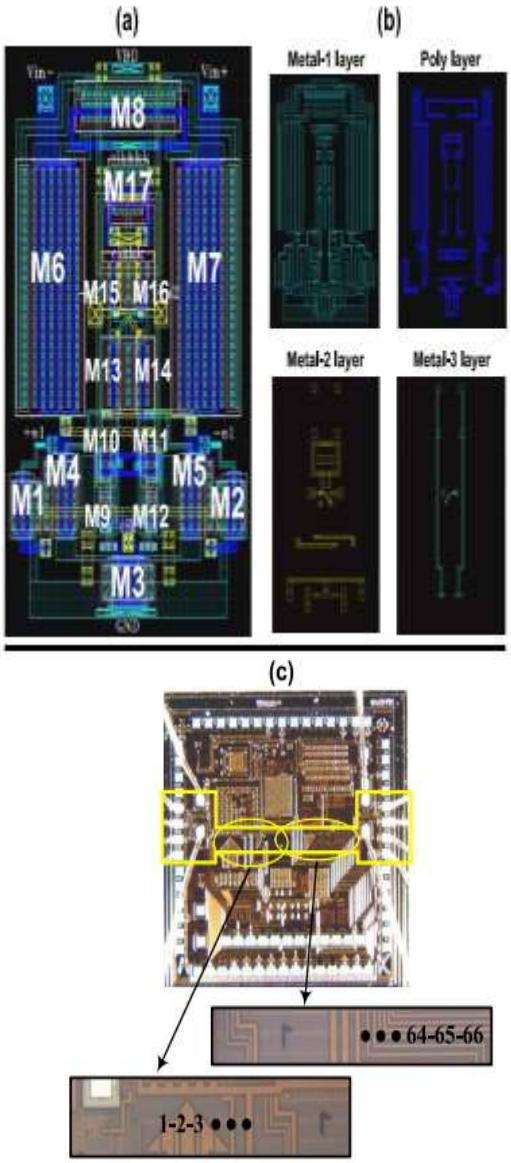
In order to confirm the benefits of the proposed comparator,the designed comparator was tested under different process(ss, tt, and ff), voltage (1.6, 1.8, and 2 V), and temperature(0°, 27°, and 70 °C) corners (PVT corners). Table III presentsthe results for 27 different corners (33 = 27). In each cell ofTable III, the top numbers represent the results considering an ideal controller (fixed 150-ps delay), while the down numberis for the proposed controller [Fig. 2(b)]. As can be seen, theoffset voltage remains about 2 mV in different corners, since the proposed controller somehow self-adjust the comparator.In fact, whenever the delay is low (e.g., VDD = 2 V, *ff*in 0 °C) the delay-line-based controller is fast forcing the comparator to work correctly. On the contrary, if the delayis high (e.g., VDD = 1.6 V, *ss*in 70 °C) the delay-line-basedcontroller is slow letting the comparator work correctly.

PARAMETERS OF THE COMPARATOR IN DIFFERENT CORNERS CONSIDERING THE IDEAL AND PROPOSED CONTROLLERS ($V_{cm} = V_{ref}/2$)

VDD = 1.6V									
Condition	T = 0°C			T = 27°C			T = 70°C		
	ss	tt	ff	ss	tt	ff	Ss	tt	ff
Delay (ps)	524 636	435 458	342 344	537 652	437 478	338 361	551 665	438 512	335 387
σV_{offset} (mV)	2.07 2.29	2.06 2.04	2.05 2.06	2.04 2.17	2.05 2.08	2.06 2.06	2.04 2.10	2.04 2.15	2.06 2.09
Power @500MHz (uW)	108 126	128 136	168 151	113 134	135 143	173 158	120 144	143 153	180 170
$\sigma V_{noise-in}$ (uV)	23 27	26 27	24 24	24 26	28 26	25 25	25 30	29 30	27 28
VDD = 1.8V									
Condition	T = 0°C			T = 27°C			T = 70°C		
	ss	tt	ff	ss	tt	ff	Ss	tt	ff
Delay (ps)	394 492	332 360	303 297	400 519	324 381	299 309	408 502	319 402	307 326
σV_{offset} (mV)	2.07 2.06	2.04 2.04	2.15 2.12	2.06 2.05	2.05 2.05	2.14 2.13	2.06 2.06	2.08 2.10	2.14 2.09
Power @500MHz (uW)	194 190	237 202	298 220	199 200	240 211	299 228	204 214	244 224	301 240
$\sigma V_{noise-in}$ (uV)	23 27	25 27	23 24	23 28	26 28	22 26	29 27	29 27	25 26
VDD = 2V									
Condition	T = 0°C			T = 27°C			T = 70°C		
	ss	tt	ff	ss	tt	ff	ss	tt	ff
Delay (ps)	317 416	307 328	296 253	322 440	302 340	293 262	332 468	299 259	292 278
σV_{offset} (mV)	2.06 2.08	2.06 2.11	2.17 2.19	2.07 2.10	2.07 2.10	2.18 2.18	2.07 2.10	2.14 2.12	2.18 2.17
Power @500MHz (uW)	314 261	374 277	457 296	314 272	377 287	463 305	315 289	378 303	468 320
$\sigma V_{noise-in}$ (uV)	25 26	23 26	25 23	26 28	22 28	25 23	30 27	26 27	24 22

As a result, the delay-line-based controller serves the comparator asa self-adjusting clock generator. The delay naturally reducesor increases in different corners. The power consumption forthe case of the proposed controller (the down

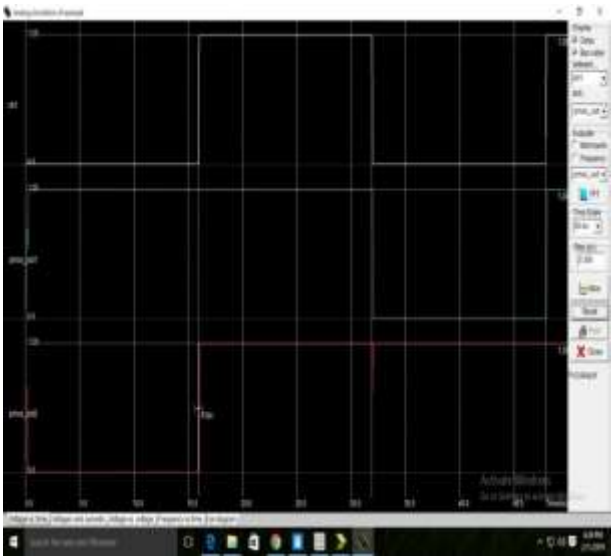
numbers) variesonly with VDD variations. In fact, in different process andtemperature corners the power consumption almost remains constant.

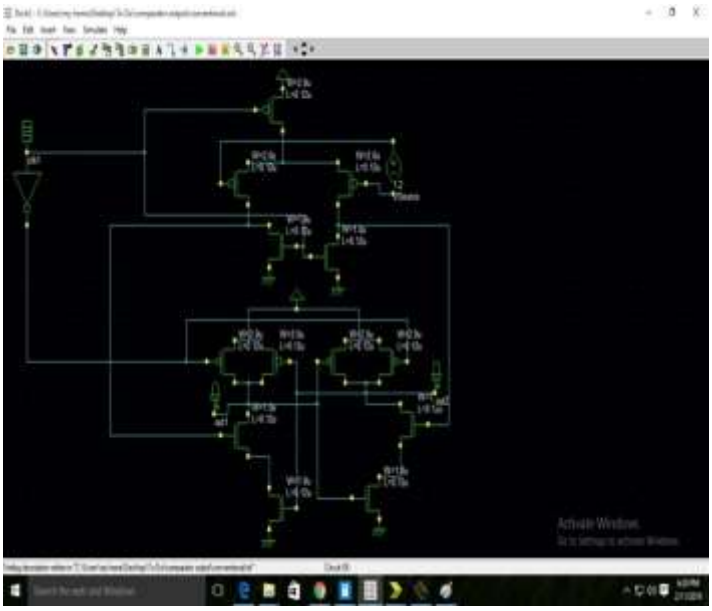


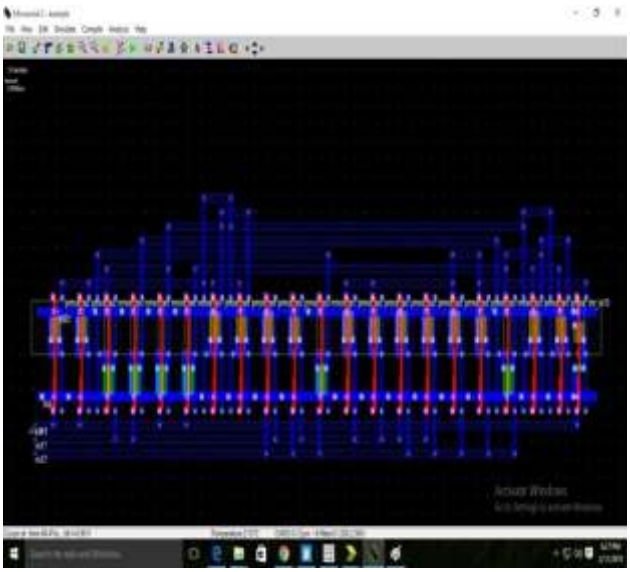
(a) Symmetric layout of the proposed comparator. (b) Differentlayers of the layout. (c) Die micrograph

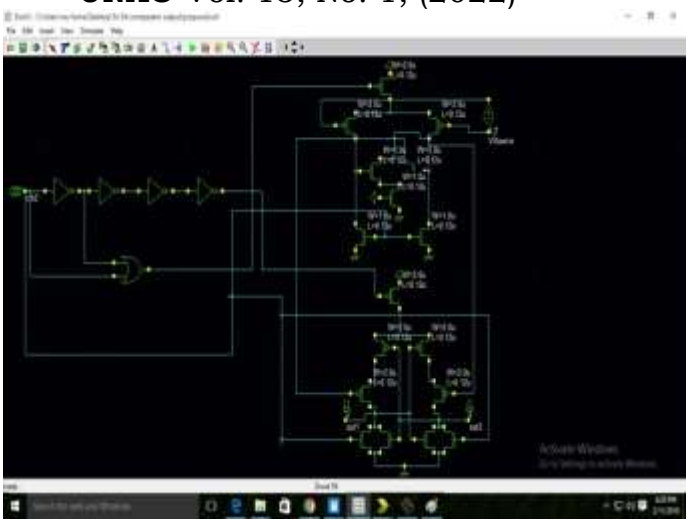
RESULTS

Conventional:

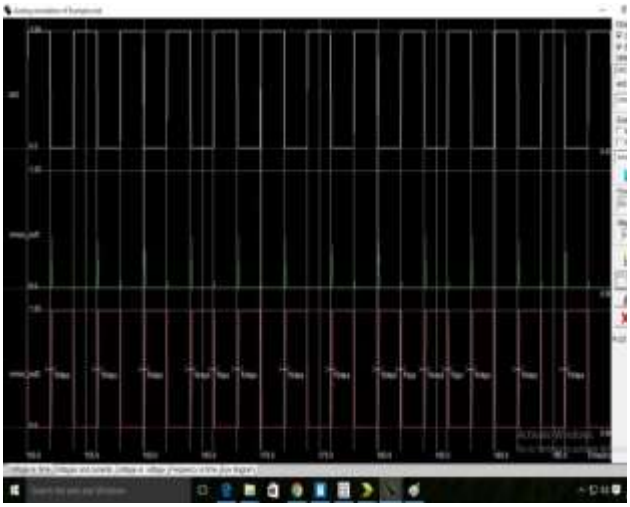


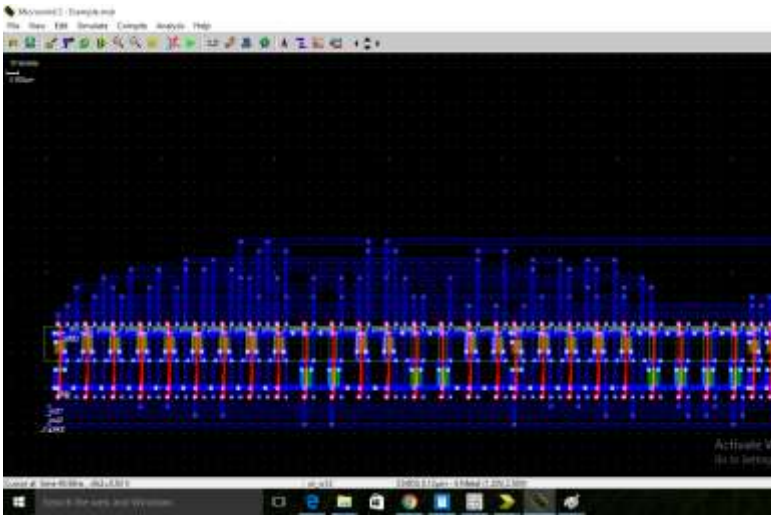






Proposed:





CONCLUSION

In the proposed comparator, pMOS latch and pMOS preamplifier in addition to a small cross coupled circuit are usedwith a special clocking pattern to adjust the preamplifier gain.

The clocking pattern provides enough preamplifier gain; since pMOS transistors are used at the input of the latch, andthe cross-coupled circuit is employed to keep the common mode voltage of the

preamplifier outputs at a low level.As a result, the speed of the comparator is increased and is constantly high for a wide input *V*cm range [Fig. 12(c)].Deactivating the preamplifier after the optimum delay reducesthe power consumption significantly. Therefore, the proposed circuit is a low-offset low-power high-speed comparator whichworks at a wide input common-mode voltage range. Analyticalmodeling, PVT corner, and post layout simulations along with silicon measurements prove the benefits of the proposedcomparator.

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